

PHP/PHB/PHD101NQ03LT

TrenchMOS™ logic level FET

Rev. 01 — 20 February 2002

Product data

1. Description

N-channel logic level field-effect power transistor in a plastic package using TrenchMOS™¹ technology.

Product availability:

PHP101NQ03LT in SOT78 (TO-220AB)

PHB101NQ03LT in SOT404 (D²-PAK)

PHD101NQ03LT in SOT428 (D-PAK).

2. Features

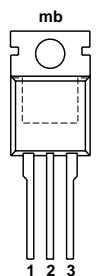
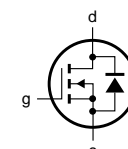
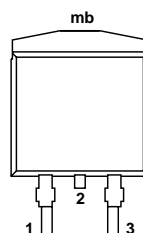
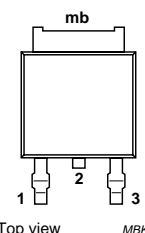
- Low gate charge
- Low on-state resistance.

3. Applications

- Optimized as a control FET in DC to DC convertors

4. Pinning information

Table 1: Pinning - SOT78, SOT404, SOT428 simplified outline and symbol

Pin	Description	Simplified outline	Symbol	
1	gate (g)	 MBK106	 MBB076	
2	drain (d)			 MBK116
3	source (s)			 Top view MBK091
mb	mounting base, connected to drain (d)			
		SOT78 (TO-220AB)	SOT404 (D²-PAK)	SOT428 (D-PAK)

[1] It is not possible to make connection to pin 2 of the SOT404 and SOT428 packages.

1. TrenchMOS is a trademark of Koninklijke Philips Electronics.



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5. Quick reference data

Table 2: Quick reference data

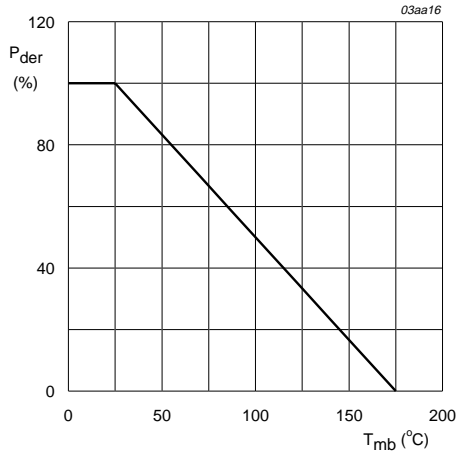
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 175 °C	-	30	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 5$ V	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C	-	166	W
T_j	junction temperature		-	175	°C
R_{DSon}	drain-source on-state resistance	$T_j = 25$ °C; $V_{GS} = 10$ V; $I_D = 25$ A	4.5	5.5	mΩ
		$T_j = 25$ °C; $V_{GS} = 5$ V; $I_D = 25$ A	5.8	7.0	mΩ

6. Limiting values

Table 3: Limiting values

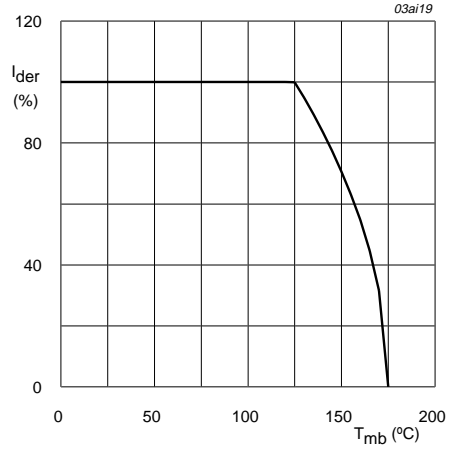
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 175 °C	-	30	V
V_{DGR}	drain-gate voltage (DC)	$T_j = 25$ to 175 °C; $R_{GS} = 20$ kΩ	-	30	V
V_{GS}	gate-source voltage (DC)		-	±20	V
V_{GSM}	gate-source voltage	$t_p \leq 50$ μs; pulsed; duty cycle 25%; $T_j \leq 150$ °C	-	±25	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 5$ V; Figure 2 and 3	-	75	A
		$T_{mb} = 100$ °C; $V_{GS} = 5$ V; Figure 2	-	75	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs; Figure 3	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Figure 1	-	166	W
T_{stg}	storage temperature		-55	+175	°C
T_j	operating junction temperature		-55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25$ °C	-	75	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs	-	240	A



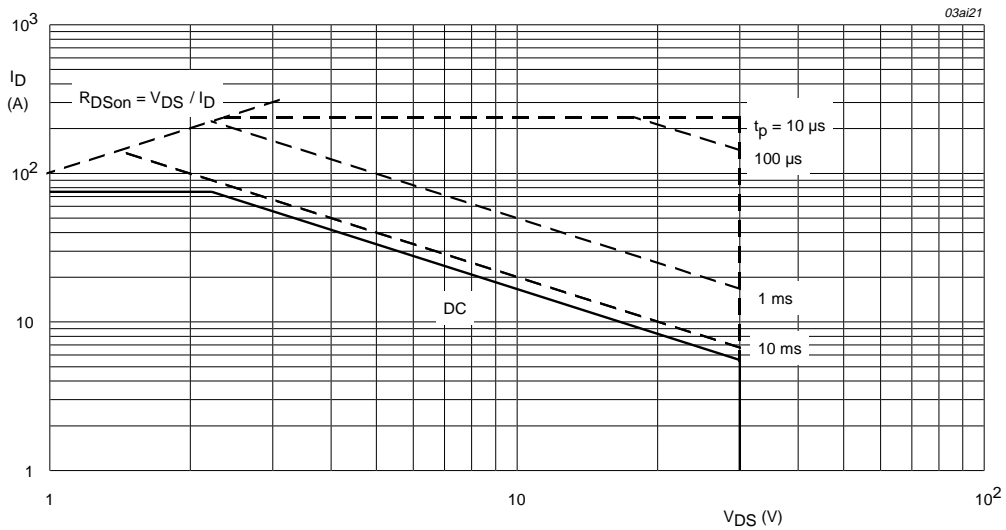
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10V.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOT78 package; vertical in still air	-	60	-	K/W
		SOT428 package; SOT428 minimum footprint; mounted on a PCB	-	75	-	K/W
		SOT404 and SOT428 packages; SOT404 minimum footprint; mounted on a PCB	-	50	-	K/W

7.1 Transient thermal impedance

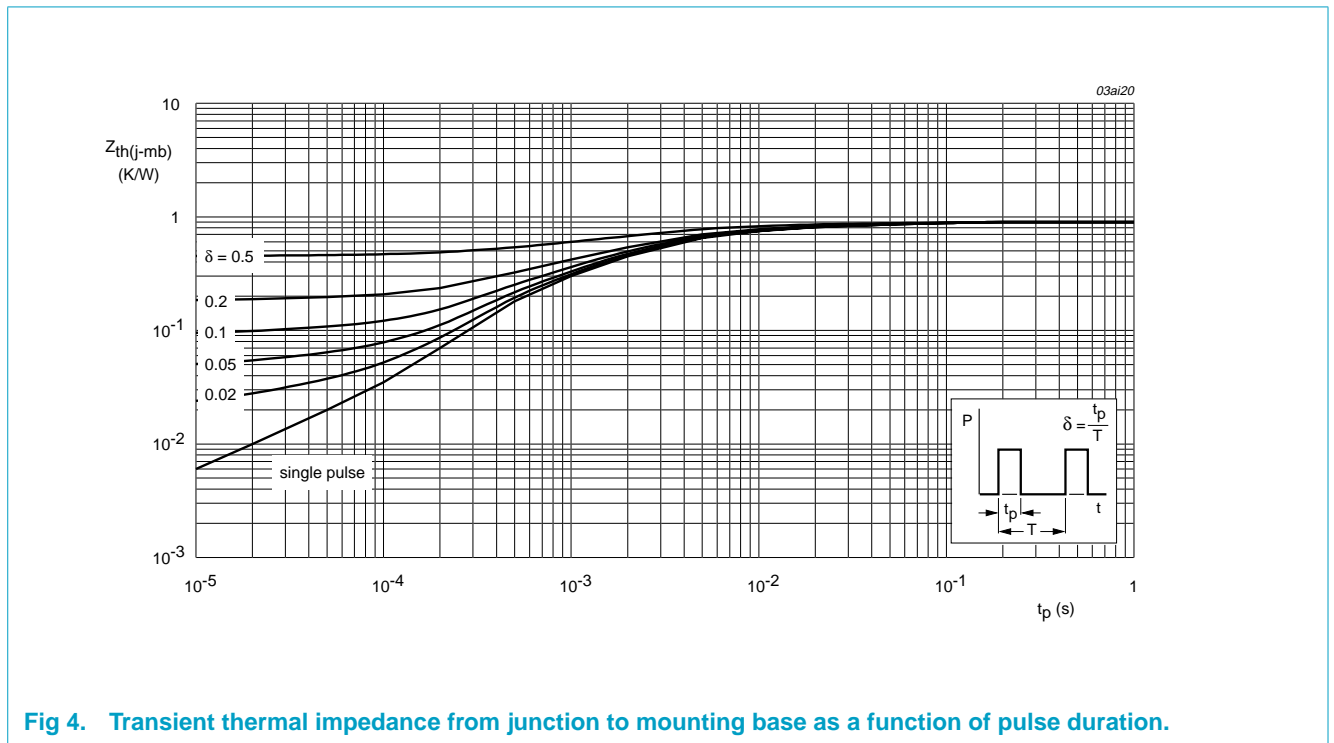
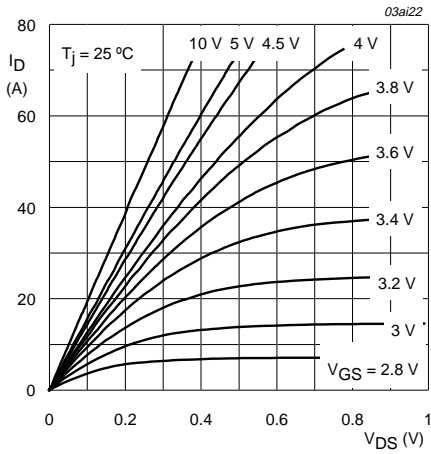


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

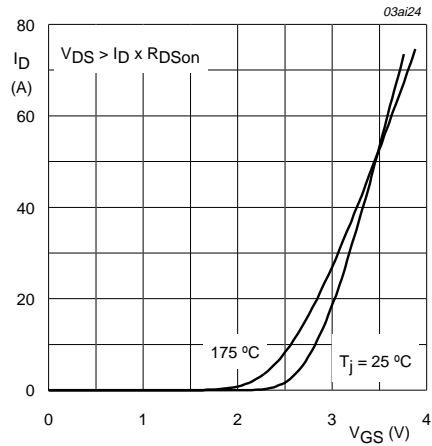
Table 5: Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V T _j = 25 °C	30	-	-	V
		T _j = -55 °C	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 T _j = 25 °C	1	1.9	2.5	V
		T _j = 175 °C	0.6	-	-	V
		T _j = -55 °C	-	-	2.9	V
I _{DSS}	drain-source leakage current	V _{DS} = 30 V; V _{GS} = 0 V T _j = 25 °C	-	0.05	1	μA
		T _j = 175 °C	-	-	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	-	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; Figure 7 and 8 T _j = 25 °C	-	5.8	7	mΩ
		T _j = 175 °C	-	10.5	12.6	mΩ
		V _{GS} = 10 V; I _D = 25 A; Figure 7 T _j = 25 °C	-	4.5	5.5	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 50 A; V _{DD} = 15 V; V _{GS} = 5 V; Figure 13	-	23	-	nC
Q _{gs}	gate-source charge		-	10.5	-	nC
Q _{gd}	gate-drain (Miller) charge		-	8	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; Figure 11	-	2180	-	pF
C _{oss}	output capacitance		-	600	-	pF
C _{rss}	reverse transfer capacitance		-	225	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 15 V; I _D = 25 A; V _{GS} = 4.5 V;	-	23	-	ns
t _r	turn-on rise time	R _G = 5.6 Ω; resistive load	-	90	-	ns
t _{d(off)}	turn-off delay time		-	37	-	ns
t _f	turn-off fall time		-	33	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 12	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V	-	37	-	ns
Q _r	recovered charge		-	33	-	nC



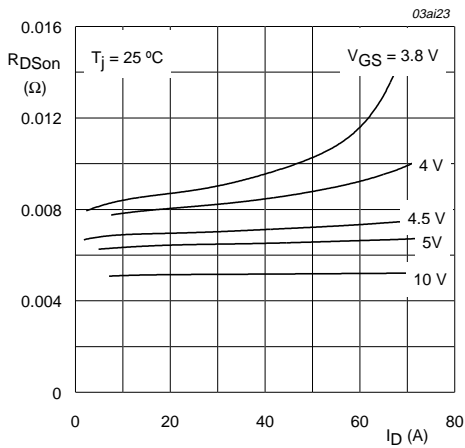
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



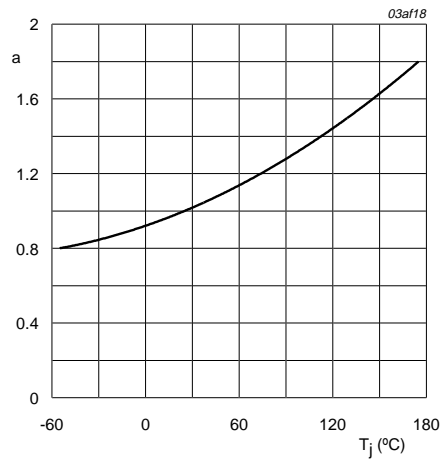
$T_j = 25\text{ °C}$ and 175 °C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



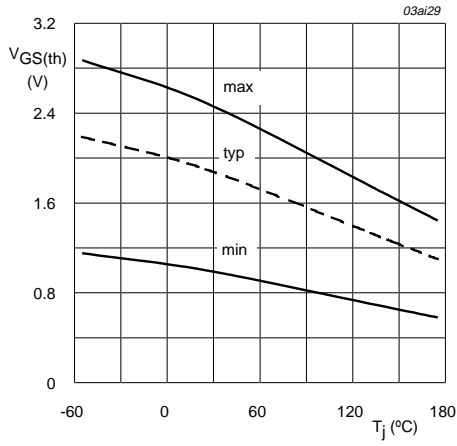
$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



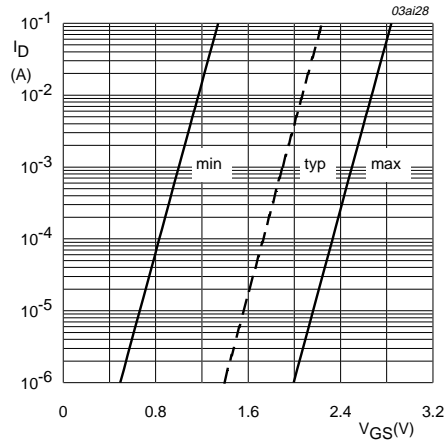
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



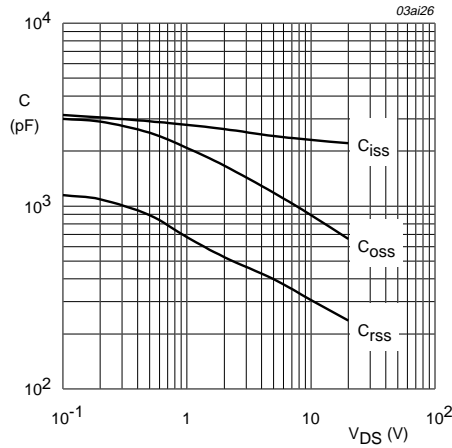
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



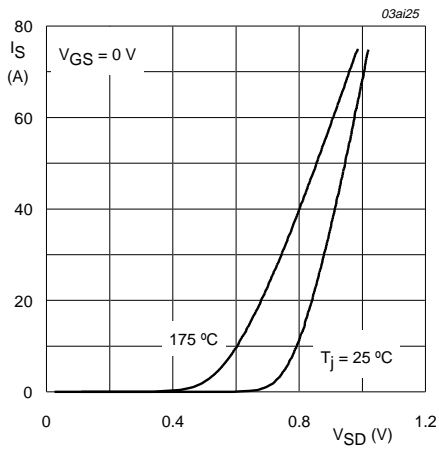
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



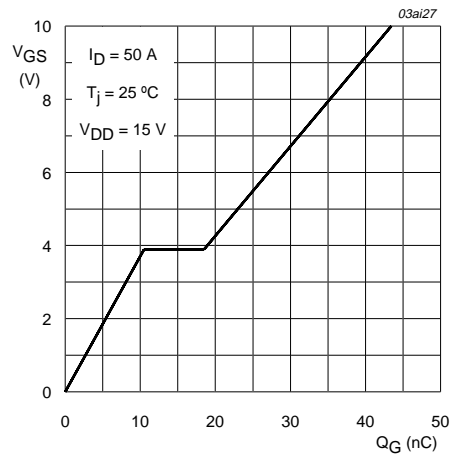
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$ and 175 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 50\text{ A}$; $V_{DD} = 15\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



Fig 14. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404



Fig 15. SOT404 (D²-PAK)

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428



Fig 16. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20020220	-	Product data; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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